IN THE CLAIMS:

Please amend claims 1, 2, 4, and 6-15, cancel claims 3 and 5, and add new claims 17 and 18 as shown in this complete set of all pending claims:

1. (Currently Amended) In a target processor having three states: a primary code execution state, a secondary code execution state, and an execution halt state, a trace apparatus comprising:

   a trigger unit responsive to user and target processor state input signals corresponding to the three states, the trigger unit generating control signals in response to the input signals;

   timing trace apparatus, the timing trace apparatus responsive to the control signals for selectively providing timing trace streams during the secondary code execution state~~, while continuing to provide timing trace streams during~~ and the primary code execution state;

   program counter and data trace apparatus, the program counter and data trace apparatus responsive to the control signals for selectively providing program counter and data trace streams during the secondary code execution state when the timing trace ~~unit~~ apparatus is providing timing trace streams during the secondary code execution state; and

   a test and debug port, the test and debug port adapted for coupling to a communication bus, the test and debug port receiving signals from and sending signals to a host processor unit,

   wherein the control signals individually enable and disable each of the timing trace apparatus and the program counter and data trace apparatus based on a current state of the target processor.

2. (Currently Amended) The trace apparatus as recited in claim 1 wherein the secondary code execution state is a background or interrupt service routine code execution state.

3. (Canceled)

4. (Currently Amended) The trace apparatus as recited in claim 1 further comprising a pipeline flattener, the pipeline flattener aligning ~~the~~ a program counter address with ~~the~~ completion of ~~the~~ an instruction, the pipeline flattener flushing instructions in response to a halt execution signal in an unprotected pipeline, the pipeline flattener halting operation in a protected pipeline.

5. (Canceled)

6. (Currently Amended) The trace apparatus as recited in claim [[5]] 1 wherein the timing trace stream can be controllably enabled during [[an]] the execution halt state.

7. (Currently Amended) A method of generating trace streams in a target processor for transmission to a host processor, the method comprising:

~~selecting one or more of a plurality of processor execution states, wherein tracing is enabled for the selected execution states and disabled for the non-selected execution states;~~

generating a timing trace stream in the target processor in response to preselected user and target processor input signals ~~such that a timing trace stream is generated while the processor executes in a given execution state only when timing tracing is enabled for that execution state~~;

when the timing trace stream is being generated, generating a program counter trace stream and a data trace stream in response to predetermined user and target processor input signals~~, such that the program counter and the data trace stream is generated while the processor executes in a given execution state only when program counter and data tracing is enabled for that execution state~~; and

sending the trace streams to the host processing unit over a communication bus,

wherein the predetermined user and target processor input signals individually enable or disable the generation of each of the timing trace stream, the program counter trace stream, and the data trace stream based on a current state of the target processor.

8. (Currently Amended) The method as recited in claim 7 further comprising including in the target processor input signals indicia of the current state of the target processor, the target processor having a primary code execution state, a secondary code execution state and an execution halt state.

9. (Currently Amended) The method as recited in claim 7 further comprising including in the target processor input signals indicia indicating whether the target processor ~~was~~ is in a protected pipeline mode of operation or in an unprotected pipeline mode of operation.

10. (Currently Amended) The method as recited in claim 7 further comprising including in the user input signals whether the timing trace stream is ~~was~~ enabled during instruction execution halts.

11. (Currently Amended) The method as recited in claim [[9]] 8 further comprising including in the user input signals ~~identifying when~~ whether the timing trace stream ~~was~~ is enabled during the secondary code execution state.

12. (Currently Amended) A processing unit comprising:

a central processing unit, the central processing unit having three states of operation, a primary code execution state, a secondary code execution state, and an execution halted state; and

trace generating apparatus including:

a program counter trace stream generation unit and a data trace stream generation unit, the program counter trace stream generation unit and the data trace generation unit responsive to control signals for generating ~~the~~ a program counter trace stream and ~~the~~ a data trace stream[[s]] respectively;

a timing trace stream generation unit, the timing trace stream generation unit responsive to control signals for generating a timing trace stream ~~in response to control signals~~;

a trigger unit responsive to user input signals and to central processing unit signals for generating ~~first and second~~ control signals controlling the timing trace generation unit, ~~and~~ the program counter trace generation unit, and the data trace generation unit, wherein the trigger unit is operable to ~~selectively~~ individually enable and disable ~~tracing~~ trace stream generation by each of the program counter trace stream generation unit, ~~by~~ the data trace stream generation unit, and ~~by~~ the timing trace stream generation unit in response to a current state of operation of the central processing unit; and

a port for applying selected trace signals to a communication bus.

13. (Currently Amended) The processing unit as recited in claim 12 wherein ~~first~~ the control signals enable the timing trace generation unit during the secondary code execution state.

14. (Currently Amended) The processing unit as recited in claim 13 wherein ~~second~~ the control signals enable the timing trace generation ~~device~~ unit, ~~and~~ the program counter trace generation unit, and the data trace generation unit[[s]] during the secondary code execution state.

15. (Currently Amended) The processing unit as recited in claim 12, wherein ~~including~~ indicia of a protected pipeline mode of operation and of an unprotected pipeline mode of operation of the central processing unit are part of the central processing unit input signals.

16. (Previously Presented) In a target processor, a trace apparatus comprising:

a trigger unit responsive to user and target processor state input signals, the trigger unit generating control signals in response to the input signals;

timing trace apparatus, the timing trace apparatus responsive to the control signals for selectively providing timing trace streams during secondary code execution;

program counter and data trace apparatus, the program counter and data trace apparatus responsive to the control signals for selectively providing program counter and data trace streams during secondary code execution when the timing trace unit is providing timing trace streams during the secondary code execution;

a pipeline flattener, the pipeline flattener aligning the program counter address with the completion of the instruction, the pipeline flattener flushing instructions in response to a halt execution signal in an unprotected pipeline, the pipeline flattener halting operation in a protected pipeline; and

a test and debug port, the test and debug port adapted for coupling to a communication bus, the test and debug port receiving signals from and sending signals to a host processor unit.

17. (New) In a target processor, a trace apparatus comprising:

a trigger unit responsive to user and target processor state input signals, the trigger unit generating control signals in response to the input signals;

timing trace apparatus, the timing trace apparatus responsive to the control signals for selectively providing timing trace streams during a secondary code execution state and a primary code execution state;

program counter and data trace apparatus, the program counter and data trace apparatus responsive to the control signals for selectively providing program counter trace and data trace streams during the secondary code execution state when the timing trace unit is providing timing trace streams during the secondary code execution state; and

a test and debug port, the test and debug port adapted for coupling to a communication bus, the test and debug port receiving signals from and sending signals to a host processor unit,

wherein the target processor has three states, the primary code execution state, the secondary code execution state, and an execution halt state; and

wherein the trigger unit is responsive to the three states to selectively enable and disable the timing trace apparatus and the program counter and data trace apparatus in accordance with a current state of processor execution; and

wherein the timing trace stream can be controllably enabled during the execution halt state.

18. (New) The processing unit as recited in claim 12 wherein the control signals enable the timing trace generation unit during the execution halted state.